REMARKS

The following remarks are submitted as a full and complete response to the outstanding Action. By this Amendment, claims 4 and 15 have been amended to more clearly set forth the present application. No new matter has been added. Accordingly, claims 1-19 are pending for consideration and submitted for reconsideration thereof.

CLAIM OBJECTIONS

The disclosure is objected to due to certain informalities.

Claim 4 has been amended to address the concerns as set forth in item 2 of the outstanding Action.

Claim 15 has been amended to correct a typographical error.

CLAIM REJECTIONS

Claims 1 and 3 are rejected under 35 U.S.C. §102(e) as being anticipated by *Hirata* (U.S. Patent No. 6,469,354).

Conventional art on ESD protection is directed to increasing or improving the function of the ESD protective circuit. For instance, the ESD protection can be improved by increasing the conduction speed or tolerance of the ESD protective circuit.

On the other hand, the present application as set forth in claims 1 and 3 takes an opposite approach to improve the ESD protection by, e.g., reducing the conduction speed of a transistor component which is not part of the ESD protective circuit. For instance, an additional pickup region is implemented to surround the source of a transistor device. If the transistor device has multi-fingers, then each source of the multi-fingers is surrounded by the additional pickup region to effectively reduce, e.g., the conduction speed of the transistor component.

By contrast, the purported pickup region in ***Hirata***, which is akin to the conventional art, merely surrounds a guard ring at the periphery of the ESD protective circuit. In other words, ***Hirata*** simply lacks any teaching or suggestion regarding the reduction of turn-on speed in the transistor component being protected by the ESD protective circuit.

Additionally, it is respectfully submitted that the application of Figs. 5, 7 and 12 of ***Hirata*** as set forth in the outstanding Action is clearly erroneous due to a mismatch relative to the first, second, third and fourth regions of claims 1 and 3. More specifically, the regions 10b and 26 do not correspond to the fourth region as set forth in claims 1 and 3, and the region 10b in Fig. 5 does not lie between the source of the first MOS transistor and the source of the second MOS transistor, and therefore cannot correspond to the fourth region of the first conductivity type recited in claim 1. Also, the region 26 of Fig. 7 is referring to an N-well, and is of a second conductivity type. Therefore, it cannot correspond to the fourth region of the first conductivity type recited in claim 1 of the present

invention. Lastly, Fig. 12 does not contain a region analogous to the fourth region of the first conductivity type.

Claims 8 and 10 are rejected under 35 U.S.C. §102(e) as being anticipated by *Hirata*.

As discussed above, the purported regions of ***Hirata*** do not correspond to the first N+, third N+ and P+ regions as presently set forth in claims 8 and 10. Regarding claim 8, the outstanding Action refers to Figs. 5, 7 and 12 of ***Hirata***.

However, in Fig. 5, the region 10b does not lie between the source of the first MOS transistor and the source of the second MOS transistor, so it cannot correspond to the P+ region disposed between the second N+ region (source) of the first MOS transistor and the third N+ region (source) of the second MOS transistor as recited in claim 8.

In Fig. 7, 26 is an N-well. As such, it cannot correspond to the to the P+ region disposed between the second N+ region (source) of the first MOS transistor and the third N+ region (source) of the second MOS transistor as recited in claim 8 of the present invention.

Fig. 12 also does not appear to contain a region analogous to the P+ region disposed between the second N+ region (source) of the first MOS transistor and the third

N+ region (source) of the second MOS transistor as recited in claim 8 of the present application.

Furthermore, as claim 10 depends from claim 8, ***Hirata*** is also inapplicable for at least the reasons stated above with respect to claim 8.

Hence, the application of Figs. 5, 7 and 12 of ***Hirata*** do not appear to correspond to the first N+, second N+, third N+ and P+ regions as presently set forth in claims 8 and 10, and in particular, regions 10b and 26 do not correspond to the P+ region as set forth in claims 8 and 10.

Claims 2, 4, 5, 7 and 15-19 are rejected under 35 U.S.C. §102(e) as being anticipated by *Hsu, et al.* (U.S. Patent No. 6,057,579, hereinafter "*Hsu*").

Hsu is also directed specifically to an ESD protective device for preventing the damaging effect of the ESD. Specifically, the wider channel length is limited to the sides of the ESD protective device to improve the turn-on uniformity of the ESD protective device.

Accordingly, ***Hsu*** also has the above-discussed deficiency with respect to ***Hirata*** regarding the reduction of conduction in the transistor component which is being protected by the ESD protective device. For instance, the wider channel length is directed to the transistor component. If the transistor component has multi-fingers, then each multi-finger

is surrounded by the wider channel length to effectively reduce, e.g., the conduction speed of the transistor component.

Claims 3 and 6 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Hsu* in view of Admitted Prior Art ("*APA*").

APA does not compensate for the above-discussed deficiency in ***Hsu*** and ***Hirata***. Therefore, claims 3 and 6 can be distinguished over ***Hsu*** and ***APA*** for the same reasons as stated above.

Claims 9, 11, 12 and 14 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Hirata* in view of *Hsu*.

It is respectfully submitted that certain portions of ***Hsu*** are erroneously referred to in items 16-19 of the outstanding Action as contained in ***Hirata***. Nonetheless, claims 9, 11, 12 and 14 are distinguishable over ***Hirata*** and ***Hsu*** for at least the same reasons as discussed above.

In view of the aforementioned amendments and accompanying remarks, claims 1-19 are now in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, the applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 50-2394

Respectfully submitted,

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